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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/690,530 | 10/23/2003 | Takayuki Kondo | 117478 | 6381 |

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| EXAMINER | |
|---|---|
| KIM, JOANNE H | |
| ART UNIT | PAPER NUMBER |
| 2883 | |

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/690,530 | KONDO, TAKAYUKI | |
| | Examiner | Art Unit | |
| | Joanne H. Kim | 2883 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-7, 12 and 19-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshimura et al. (U.S. Patent No. 6,693,736, hereinafter "Yoshimura").

Regarding claim 1, Yoshimura discloses an optical interconnection circuit between chips comprising: a substrate; a first micro tile element having a light emitting function provided on the substrate; a second micro tile element having a light receiving function provided on the substrate; an optical waveguide optically connecting the first micro tile element and the second micro tile element with each other, and including an optical waveguide member formed on the substrate, wherein the optical waveguide is in contact with and covers the first micro tile element such that at least a light emitting part of the first micro tile element is covered, and is in contact with and covers the second micro tile element such that at least a light receiving part of the second micro tile element is covered; and an electrode provided on the substrate and electrically connected to at least one of the first micro tile element and the second micro tile element (Figs. 30B, 35, 40, 45, 50, and 55; column 13, lines 1-4, 23-24 and 29-30;

column 14, lines 44-49 and 66-67; column 15, lines 1-11, 41-44, and 52-56; column 27, lines 24-27; column 28, lines 10-13; and column 31, lines 57-67).

Regarding claims 2-7 and 12, Yoshimura discloses that the electrode is a bonding pad which is a wiring electrode for an integrated circuit chip mounted onto the substrate, the electrode is a bonding pad in a case of an integrated circuit chip being flip-chip mounted onto the substrate (Figs. 30B, 41-43 and 50). Yoshimura also discloses that the optical interconnection circuit further includes a bump composed of a convex conductive member and formed on the integrated circuit chip electrically connected to at least one of terminals of the integrated circuit chip and bonded to the electrode (Fig. 50; and column 14, lines 11-14); the integrated circuit chip includes at least a plurality of integrated circuit chips which are mounted onto the substrate and a signal is transmitted among the plurality of integrated circuit chips via at least the first micro tile element, the second micro tile element, and the optical waveguide (Figs. 41 and 42); the second micro tile element includes at least a plurality of second micro tile elements optically connected to a single of the optical waveguide (Figs. 41-43); the first micro tile element emits light which is to be a clock signal (column 15, line 39); and the optical waveguide is treated to prevent extraneous light from entering the optical waveguide (column 9, lines 3-6).

Regarding claims 19-20, Yoshimura discloses an electro-optical device comprising the optical interconnection circuit. Further, it is inherent that the optical interconnection circuit is a part of electronic equipment.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 8-11 and 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshimura.

Regarding claim 8, Yoshimura discloses the optical interconnection circuit comprising the first micro tile element having a light emitting function, the second micro tile element having a light receiving function, and the waveguide optically connecting the first micro tile element and the second micro tile element formed on the substrate. Further, Yoshimura discloses that the optical interconnection circuit includes an integrated circuit to time control and an integrated circuit to provide driving being mounted onto the substrate as the integrated circuit chip; and the optical waveguide including at least one optical waveguide which is provided between the integrated circuit to time control and the integrated circuit to provide driving (Fig. 42; and column 15, lines 12-24 and 35-40).

Yoshimura does not explicitly disclose that the substrate is an element of a flat panel display.

It would have been obvious to one of ordinary skill in the art that the substrate is an element of a flat panel display since it was known in the art that the optical circuit

such as that taught by Yoshimura is used in optical display devices such as a flat panel display.

The motivation would have been to provide improved viewing angle.

Regarding claims 9-11, Yoshimura discloses that the integrated circuit to provide driving including at least a plurality of integrated circuits to provide driving are mounted onto the substrate and at least a single of the optical waveguide is provided for each of the integrated circuits to provide driving; the integrated circuit to time control is electrically connected to the first micro tile element which corresponds to the integrated circuit to provide driving mounted onto the substrate; and the integrated circuit to provide driving is electrically connected to at least one of the second micro tile element (column 15, lines 12-39).

Regarding claim 13, Yoshimura discloses the optical interconnection circuit comprising the first micro tile element including at least a plurality of fist micro tile elements (Figs. 41 and 42; and column 30, lines 54-55).

Yoshimura does not explicitly disclose that the plurality of the first micro tile elements emit light having at least two kinds of wavelengths to the optical waveguide.

It is well known that an array of light emitting elements, such as LDs, is used to simultaneous transmit different wavelength signals in a single waveguide.

Accordingly, it would have been obvious to one of ordinary skill in the art that the plurality of first micro tile elements emit light having at least two kinds of wavelengths to the waveguide since it was known in the art.

Regarding claim 14, Yoshimura discloses that the optical waveguide includes a light scattering mechanism scattering light, which is installed in the vicinity of at least one of the first micro tile element and the second micro tile element (Fig. 64; and column 34, lines 37-51).

Regarding claims 15-18, Yoshimura discloses that the optical waveguide includes the light scattering mechanism.

Yoshimura does not specifically disclose that the light scattering mechanism is composed of a resin into which a light scattering particle is mixed; a resin of which a surface is processed to include an irregularity; the optical waveguide member of which at least one of the line width and the height differ from the other; or one of a dome-shaped resin and a glass in which a light scattering parcel is dispersed.

It is well known to use a resin mixed with a light scattering particle as a scattering means in optical devices. Further, it is well known that irregularity of a surface causes scattering of light.

It would have been obvious to one of ordinary skill in the art to use the light scattering mechanism composed of a resin mixed with a light scattering particle, a resin in which a light scattering particle is dispersed, a resin of which a surface includes irregularity, or the optical waveguide including a surface having irregularity (i.e., at least one of the line width and the height differ from the other) since it was known in the art. Further, it would have been obvious to one of ordinary skill in the art to use a dome-shaped resin since it would have been an obvious matter of design choice since such a modification would have involved a mere change in the shape of a component.

***Response to Arguments***

5. Applicant's arguments filed February 28, 2005 have been fully considered but they are not persuasive.

Applicant states, in page 8,

> "In Yoshimura 736, then, the optical waveguide is described to be provided on or in a substrate, and an optical element is provided on the optical waveguide or at the same level as the optical waveguide. For example, Yoshimura 736 describes that the optical waveguide is embedded in the substrate while the optical element (LD) is provided on the substrate. See Figure 43. Thus, contrary to the structure of the optical interconnection circuit recited in claim 1, Yoshimura 736 fails to teach or suggest an optical waveguide that covers first and second micro tile elements such that at least the light emitting part of the first micro tile element and at least the light receiving part of the second micro tile element are covered. In no embodiment s described in Yoshimura 736 is the optical waveguide provided to cover the optical elements in this manner."

However, in addition to disclosing that the optical element is provided on the optical waveguide or at the same level as the optical waveguide, Yoshimura discloses that the light receiving element and the light emitting element may be formed below the waveguide (Figs 40, 45 and 50; column 13, lines 1-4; column 14, lines 44-49; and column 15, lines 52-56). That is, in contrast to the Applicant's statement, Yoshimura does teach an optical waveguide that covers first and second micro tile elements such that at least the light emitting part of the first micro tile element and at least the light receiving part of the second micro tile element are covered.

***Conclusion***

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joanne H. Kim whose telephone number is (571) 272-2139. The examiner can normally be reached on 8:30 a.m. to 5:00 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank G. Font can be reached on (571) 272-2415. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joanne H. Kim
Examiner
Art Unit 2883

jhk/FGF

Frank G. Font
Supervisory Patent Examiner
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